## REMARKS

This Amendment and Response is filed in reply to the Office Action dated March 20, 2003. In this Response, Applicant amends claim 16 to more explicitly state the inherent features of the claim. Support for the amendments can be found throughout the originally filed disclosure. Amendments to the claims are not an acquiescence to any of the rejections. Furthermore, silence with regard to any of the Examiner's rejections is not an acquiescence to such rejections. Specifically, silence with regard to Examiner's rejection of a dependent claim, when such claim depends from an independent claim that Applicant considers allowable for reasons provided herein, is not an acquiescence to such rejection of the dependent claim(s), but rather a recognition by Applicant that such previously lodged rejection is moot based on Applicant's remarks and/or amendments relative to the independent claim (that Applicant considers allowable) from which the dependent claim(s) depends. Applicant reserves the option to further prosecute the same or similar claims in the instant or a subsequent application. Upon entry of the Amendment, claims 1-20 are pending in the present application.

The issues of the March 20, 2003, Office Action are presented below with reference to the Office Action.

With regard to the Office Action, "Response to Arguments," paragraphs 1-6: Applicant thanks Examiner for the consideration of the previously filed Response; however, as provided herein, Applicant respectfully disagrees with Examiner's characterization of the prior art with respect to Applicant's claims.

With regard to the Office Action, "Claim Rejections - 35 U.S.C. 102," paragraphs 2-5: The Examiner rejected Applicant's independent claim 15 based on 35 U.S.C. 102(b) based on Fazakerly et al. (U.S. 4,208,635).

Applicant's independent claim 15 includes both a PLL, and a detection circuit. Examiner contends, Page 3, Office Action, that the PLL is items 10, 12, and 14 of Fazakerly et al., Figure 1. Examiner also contends that the same item 10 of Fazakerly et al., Figure 1, is the distinct "detection circuit" of Applicant's independent claim 15. Applicant claimed the PLL *separate from* the detection circuit as such elements are *distinct*. Examiner's contention that Fazakerly et

al.'s phase detector 10 can be *both* the claimed PLL *and* the claimed detection circuit is an improper rejection of Applicant's independent claim 15, for as provided herein, such elements are not the same, but rather, in accordance with basic claim construction, distinct claim elements. Applicant thus traverses Examiner's rejection of independent claim 15 based on 35 U.S.C. 102(b), and considers independent claim 15 to be allowable.

With regard to the Office Action, "Claim Rejections - 35 U.S.C. 102," paragraphs 6-7: Examiner rejected claims 16-20 based on 35 U.S.C. 102(e) and Richards et al. (U.S. 6,178,207).

Applicant amends independent claim 16 to more explicitly state the inherent features of previously provided independent claim 16. Independent claim 16 thus recites detecting a failure of a clock source, *where the clock source is coupled to an input of a phase-locked loop*, and *in response to said failure of said clock source*, said control signal altering a time constant within said PLL. Examiner points to Figure 12, the Digital PLL, item 12, as the PLL. Applicant directs Examiner to Column 11, lines 16-40, and Richards et al.'s Figure 12, which indicate that the input to the digital PLL, or item 1202, is "message data...in the I-Q format over input lines 1210." Richards et al.'s I-Q message data input to the PLL is *not* the same as Applicant's clock source input to a PLL. Because Richards et al. do not teach a clock source as an input to the PLL, as provided in the last Response, Richards et al. also do not teach Applicant's claimed "detecting a failure of the clock source [to a PLL]," and accordingly, Richards et al. also cannot teach Applicant's claimed feature of *in response to said failure of said clock source, said control signal altering a time constant within said PLL.*

Because Richards et al. fail to teach several elements of Applicant's independent claim 16, Applicant traverses Examiner's rejection of Applicant's independent claim 16 based on 35 U.S.C. 102(e), and Applicant considers independent claim 16 to be allowable. Applicant also considers dependent claims 17-20 to be allowable as depending from an allowable base claim.

With regard to the Office Action, paragraphs 8-23. The Examiner rejected claims 1-14 based on 35 U.S.C. 103(a) based on Bedrosian (U.S. 5,740,211).

As Examiner knows, based at least on MPEP 2143, a prima facie case of obviousness under 35 U.S.C. 103(a) requires (1) a suggestion or motivation in the references themselves or generally known in the art, to combine the references, (2) a reasonable expectation of success to

combine, and (3) a teaching, via the combination, of all the claimed limitations. Examiner provides one reference, Bedrosian, in rejecting independent claims 1 and 14.

In paragraph 10 of the present Office Action, page 5, Examiner correctly states "Bedrosian does not teach this," in referring to Applicant's claimed feedforward circuitry coupled to the clock detection circuit output, where the feedforward circuitry selectively couples at least one circuit element to the feedback filter circuit *of the PLL*, where the selective coupling is controlled by the clock detection circuit output. Examiner paraphrases In re Japikse as support for the rejection, but Examiner fails to recognize the obligations of the many recent and pertinent cases that provide the basis to establish a prima facie case of obviousness under 35 U.S.C. 103(a).

Applicant notes that because Bedrosian uses, as noted by Examiner, a configuration of components to selectively couple a feedforward and a feedback filter, a significant alteration of Bedrosian is required to provide the feature Applicant's independent claims 1 and 14 that includes clock detection circuit controlling a selective coupling of at least one circuit element to a feedback filter circuit *of the PLL*. Because Examiner fails to provide a motivation for such redesign of Bedrosian, Examiner also thus fails to provide reasonable expectation of success of such design. It is clear, and admitted by Examiner as provided herein, that Bedrosian alone does not include all the elements of Applicant's independent claims 1 and 14. Accordingly, Examiner fails to provide a prima facie case of obviousness under 35 U.S.C. 103(a) for failing to provide any of the elements as required at least under MPEP 2143, and thus, Examiner's rejection is improper. Applicant traverses Examiner's rejection, and considers independent claims 1 and 14 to be allowable. Dependent claims 2-13 are also allowable as depending from an allowable base claim.

**Conclusion**

Applicant considers the Response herein to be fully responsive to the referenced Office Action. Based on the above Remarks, it is respectfully submitted that this application is in condition for allowance. Accordingly, allowance is requested. If there are any remaining issues or the Examiner believes that a telephone conversation with Applicant's attorney would be helpful in expediting the prosecution of this application, the Examiner is invited to call the undersigned at 617-832-1241.

Respectfully submitted,

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Kevin A. Oliver
Reg. No. 42,049

Foley Hoag LLP
World Trade Center West
155 Seaport Boulevard
Boston, MA 02210

Phone: 617-832-1000
Fax: 617-832-7000